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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,489	04/15/2004	Frederic Reblewski	003921.00008	6574

22907 7590 07/28/2006

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,489	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been presented for examination based on the application filed on 15th April 2004.

Claim Objections

2. The claims as presented may have possible obvious type Double Patenting related to first second and third interconnect networks against U.S. Patent Nos. 5907697, 6594810, 6647362, 6947882.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 14 recites:

> In a multi-stage reconfigurable interconnect network of a logic simulation *system*, a *method* comprising routing an output from each of a plurality of simulation processors through N physical reconfigurable interconnect stages so as to effectively provide a data path for each output having greater than N reconfigurable interconnect stages.

It is unclear from the claim definition if the statutory category of the claim is a method or a system. MPEP 2106: Patentable Subject Matter – Computer Related Inventions states:

> The claims define the property rights provided by a patent, and thus require careful scrutiny. The goal of claim analysis is to identify the boundaries of the protection sought by the applicant and to understand how the claims relate to and define what the applicant has indicated is the invention. Office personnel must first determine the scope of a claim by thoroughly analyzing the language of the claim before determining if the claim complies with each statutory requirement for patentability. See In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998) ("[T]he name of the game is the claim.").
> Office personnel should begin claim analysis by identifying and evaluating each claim limitation. For processes, the claim limitations will define steps or acts to be performed.
> For products, the claim limitations will define discrete physical structures or materials.
> Product claims are claims that are directed to either machines, manufactures or compositions of matter. The discrete physical structures or materials may be comprised of hardware or a combination of hardware and software.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-14 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,574,388 issued to Barbier et al (Barbier hereafter).

   Regarding Claim 1

   Barbier teaches in a logic simulation system (Barbier: Fig.1 col.3 Lines 49-61), a reconfigurable interconnect network (Barbier: Fig.3 & 4a, Col.45 Lines 16-26) comprising a plurality of simulation processors (Barbier: Fig. 3 & 8-10 – Matrix Board having Logic Elements (LE) as simulation processors); a first reconfigurable interconnect stage configurable to receive outputs from the simulation processors (Barbier: Fig 3 & 4a –Stage 0); a second reconfigurable interconnect stage configurable to-receive outputs from the first reconfigurable interconnect stage (Barbier: Fig. 3 & 4a Stage 1 & 2 from Stage 0); and a third reconfigurable interconnect stage configurable to receive outputs from the second reconfigurable interconnect stage (Barbier: Fig.3 Element 114 a), and further configurable to provide outputs to inputs of the second reconfigurable interconnect stage (Barbier: Fig.3 Element 114 b).

Regarding Claim 2

Barbier teaches the second reconfigurable interconnect stage is further configurable to provide outputs to inputs of the simulation processors (Barbier: Fig.3 Element 104 to 102).

Regarding Claim 3

Barbier teaches further including a memory coupled to the second reconfigurable interconnect stage (Barbier: Fig.3), the second reconfigurable interconnect stage being dynamically configured in accordance with a content of the memory (Barbier: Fig.3 & 4a, Col.5 Lines 16-26).

Regarding Claim 4

Barbier teaches a logic simulation system (Barbier: Fig.1 col.3 Lines 49-61), a reconfigurable interconnect network (Barbier: Fig.3 & 4a, Col.45 Lines 16-26) a plurality of clusters, each cluster including plurality of simulation processors (Barbier: Fig.3, Fig.6a and Fig.10). Claim 4 further discloses similar limitations as claim 1 and is rejected for the same reasons.

Regarding Claim 5

Barbier teaches a second reconfigurable interconnect stage is further configurable to provide outputs back to inputs of the simulation engines of the clusters (Barbier: Fig.3 Element 104 to 102; also Fig.6a).

Regarding Claim 6

Claim 6 has similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 7

Claim 7 has similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 8

Claim 8 is identical to claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 9

Barbier teaches outputs of the second reconfigurable interconnect stage are coupled to the inputs of the third reconfigurable interconnect stage using a butterfly topology (Barbier: Fig.7).

Regarding Claim 10

Barbier teaches the second and third reconfigurable interconnect stages are each a plurality of crossbars (Barbier: Fig.3, 4a; 6b).

Regarding Claim 11

Claim 11 discloses a system that is taught by Barbier (Barbier: Col.1 Lines 10-12). Claim 11 further discloses similar limitations as claim 1 and is rejected for the same reasons. Please also see the Fig.4b for third routing the output back through the first reconfigurable interconnect stage where the I/O are sent back to the first stage (Barbier: Col.5 Lines 39-48).

Regarding Claim 12

Barbier teaches prior to the step of first routing, routing the output from the first simulation processor through a third reconfigurable interconnect stage (Barbier: Fig.3 Element 102 to 104 to 114b).

Regarding Claim 13

Barbier teaches first configuring the first reconfigurable interconnect stage, prior to the step of first routing, according to a first configuration; and second configuring the ~~first~~ [sic] *second* reconfigurable interconnect stage, prior to the step of third routing and after the step of first routing, according to a second configuration (Barrier: Col.5 Lines 16-26).

Regarding Claim 14

Barbier teaches a multi-stage reconfigurable interconnect network of a logic simulation system, a method comprising routing an output from each of a plurality of simulation processors through N physical reconfigurable interconnect stages so as to effectively provide a data path for each output having greater than N reconfigurable interconnect stages (Barbier: Fig.3 Input to XBAR = 64, output from XBAR =512).

Conclusion

5. All claims are rejected.
6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
7. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Wednesday, July 12, 2006

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